

Fig. 1

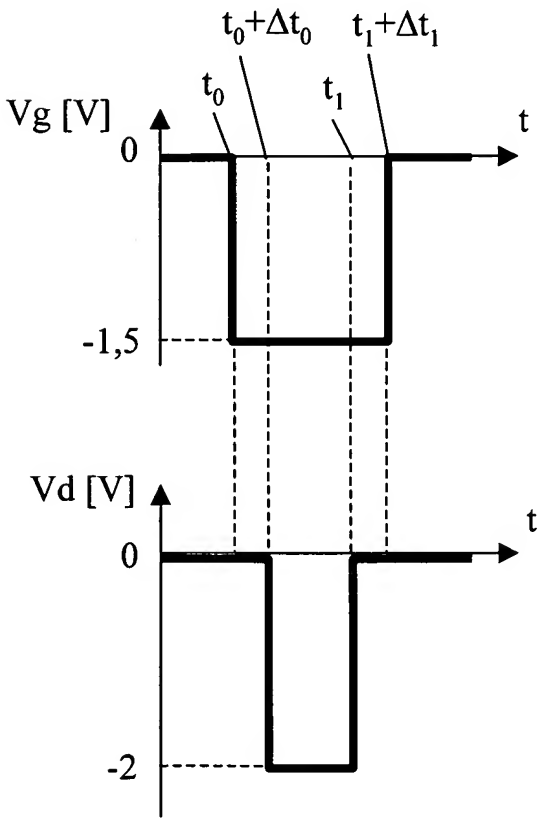


Fig. 2

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Fig. 5b

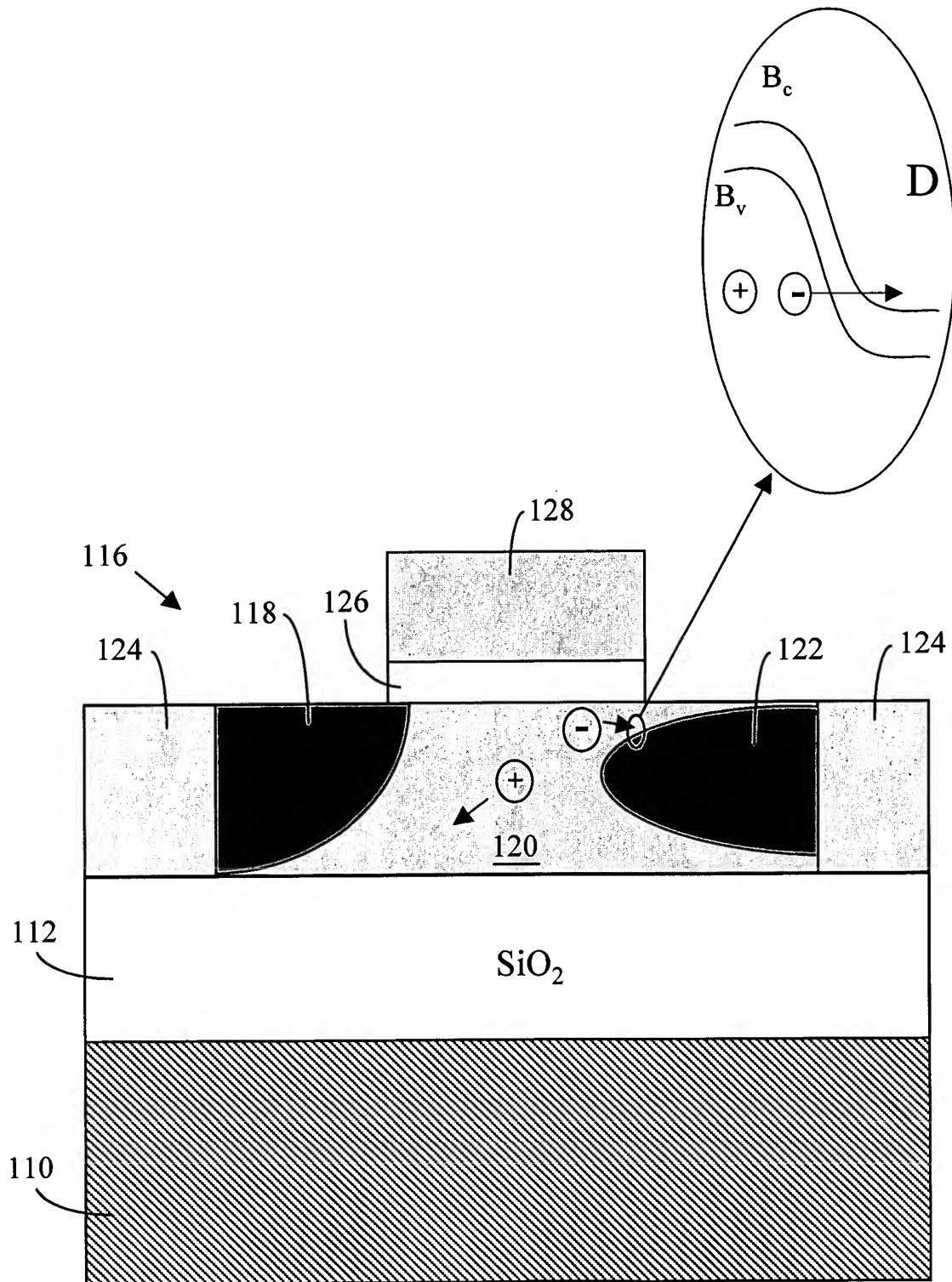


Fig. 5a

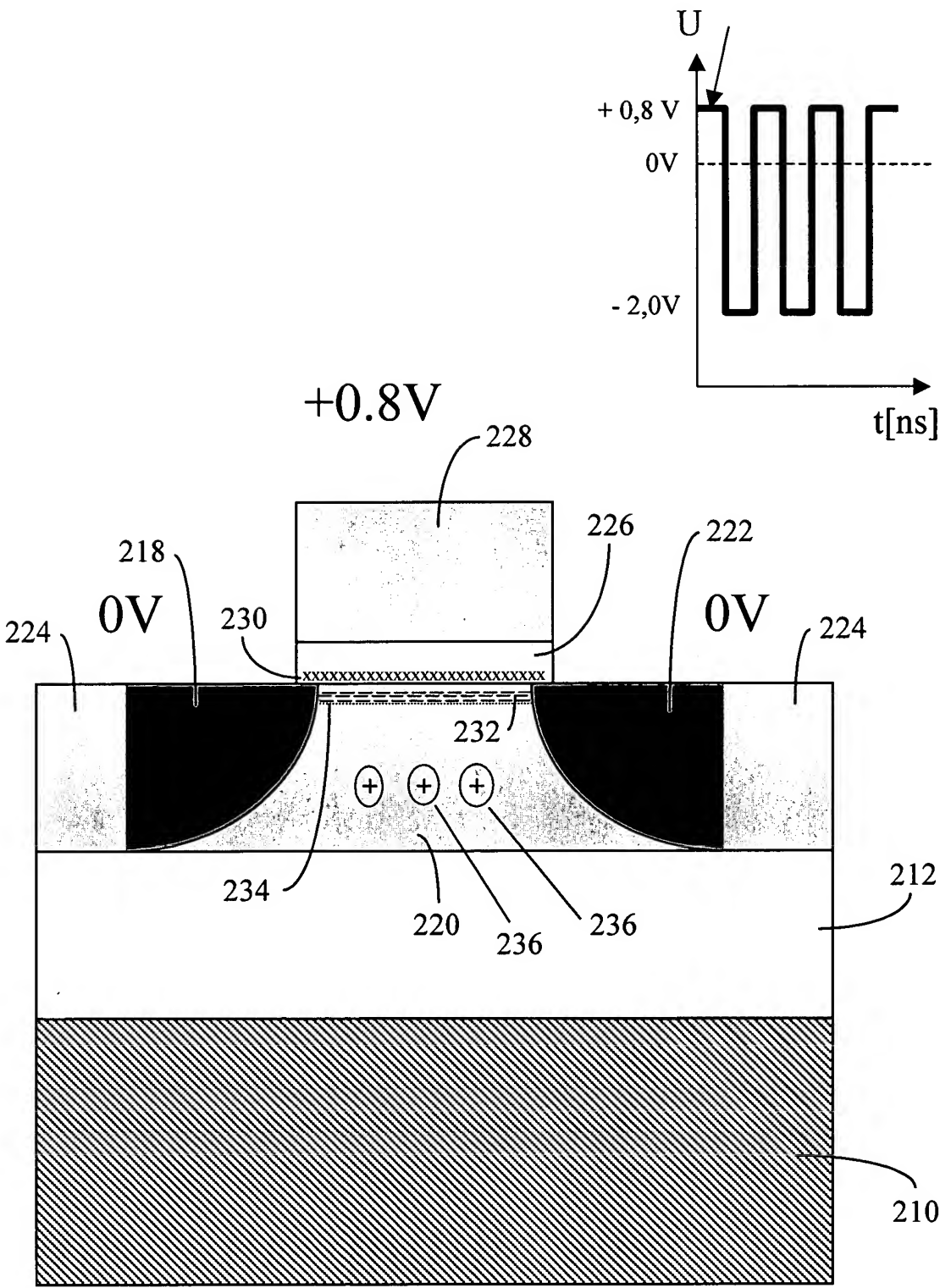


Fig. 6a

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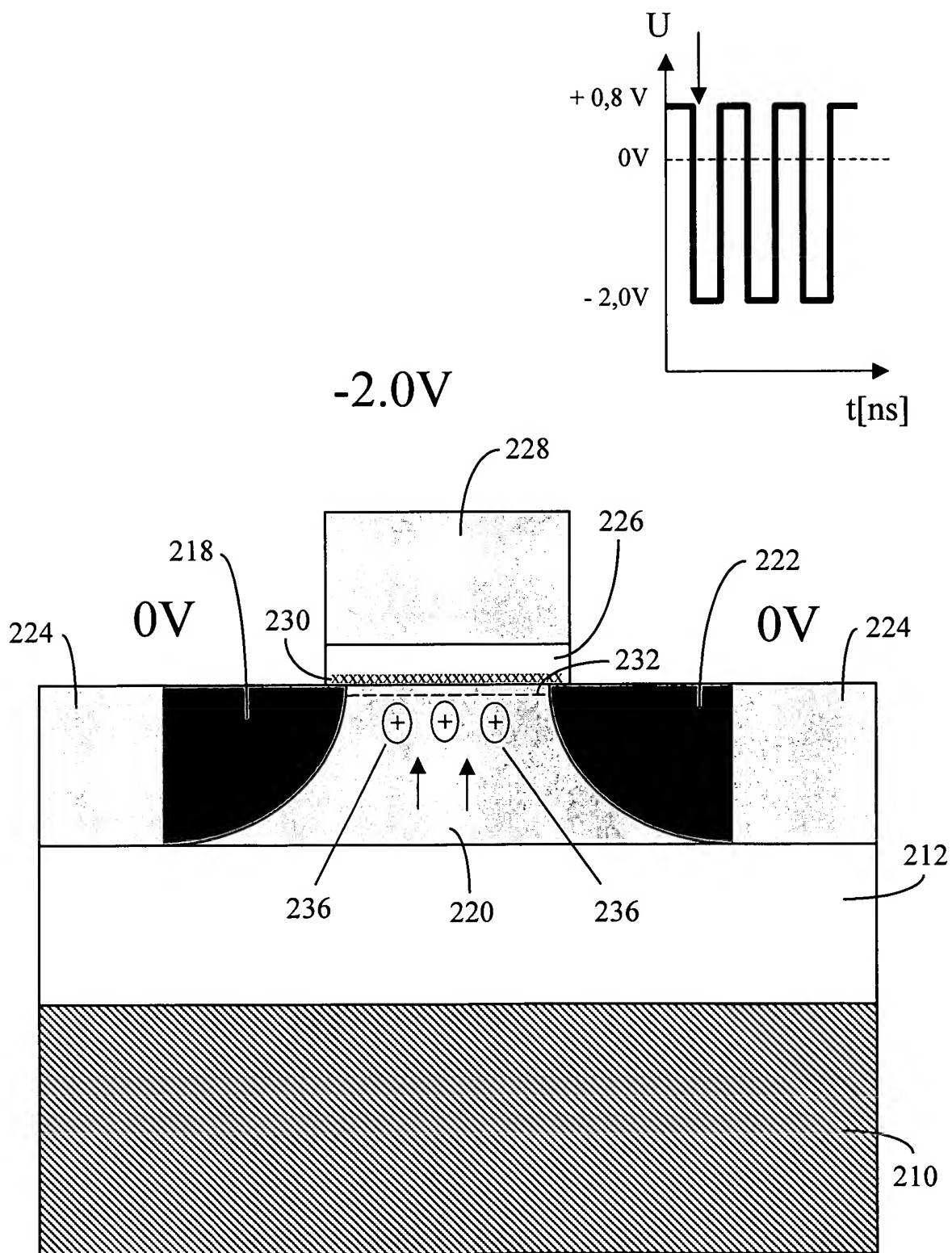


Fig. 6b

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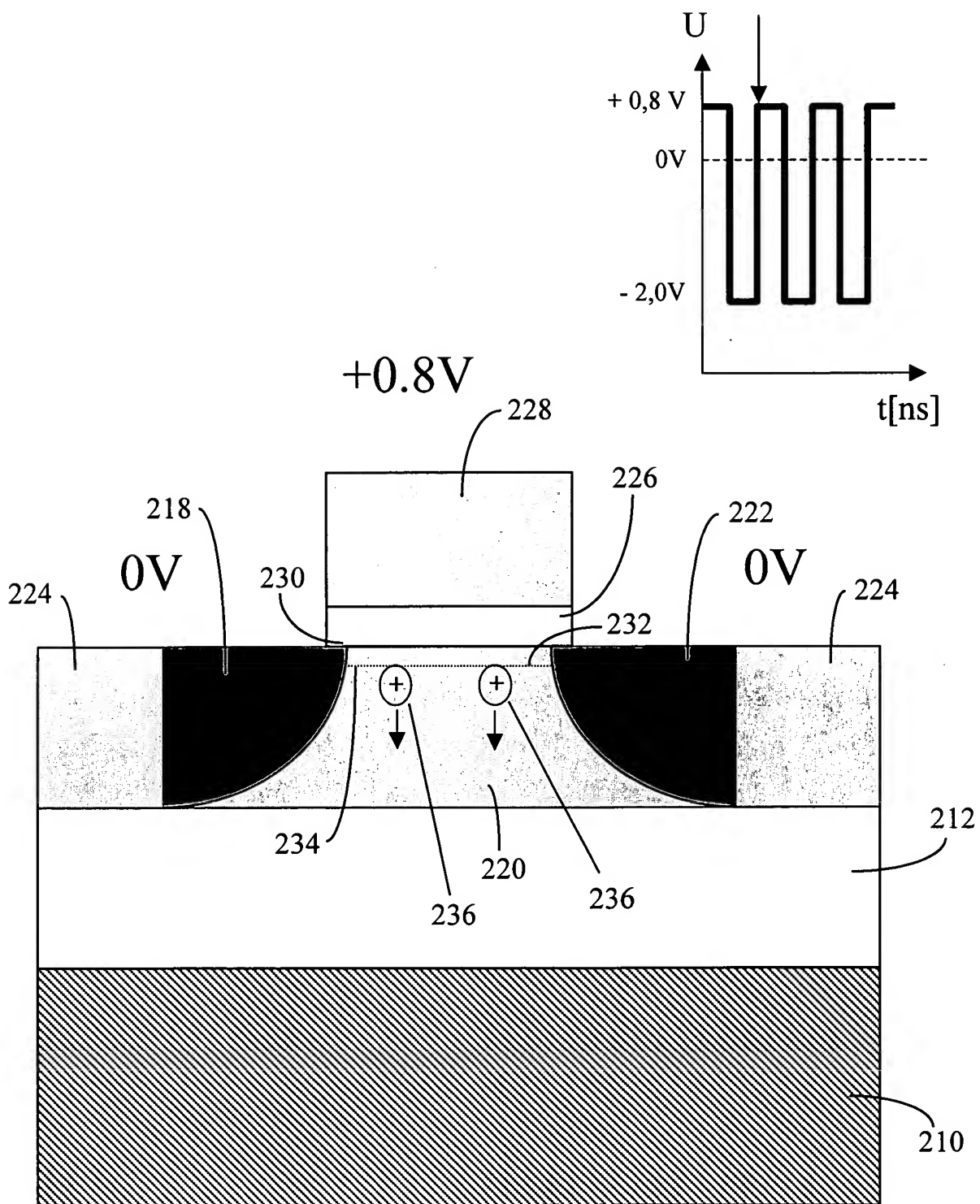


Fig. 6c

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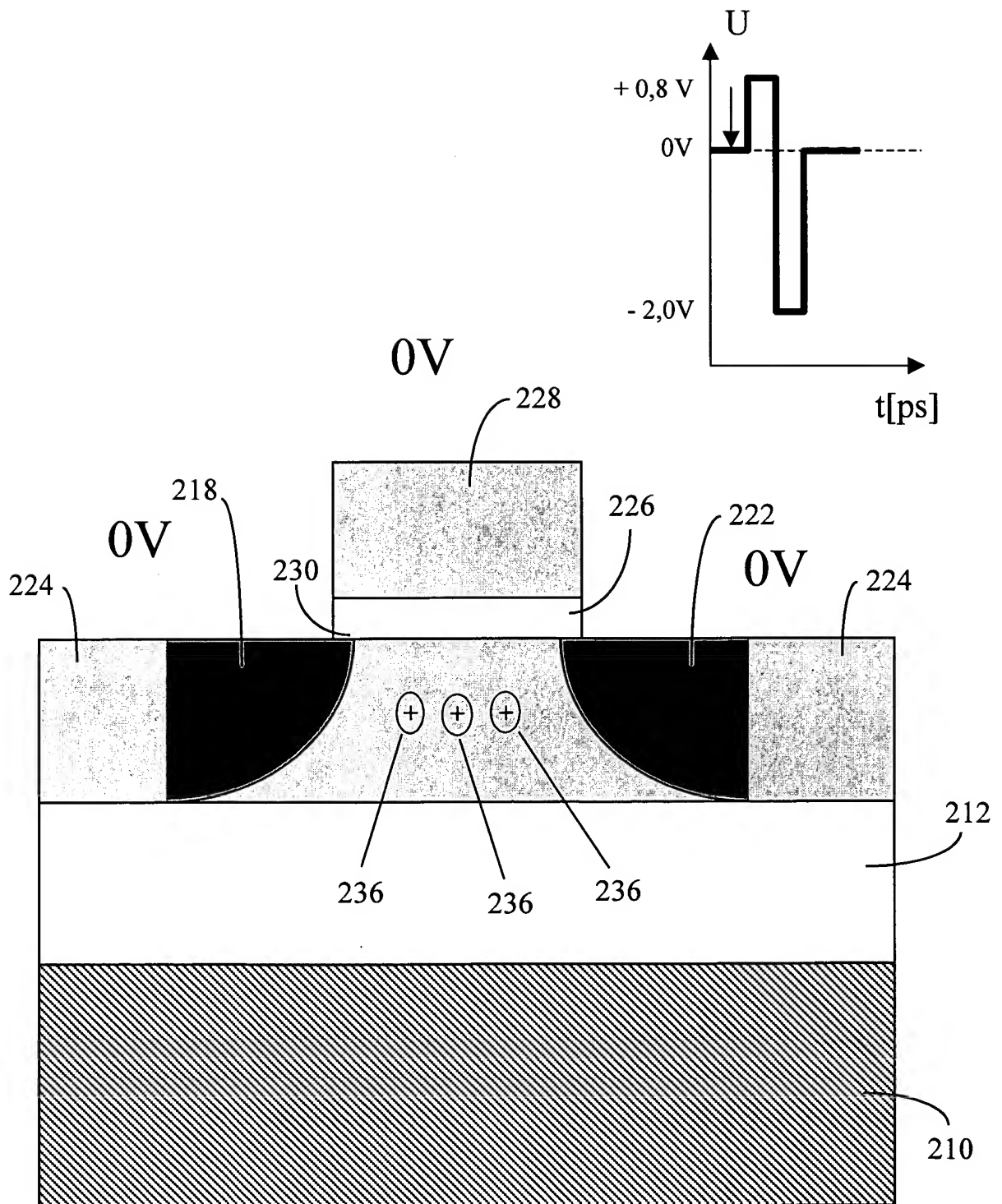


Fig. 7a

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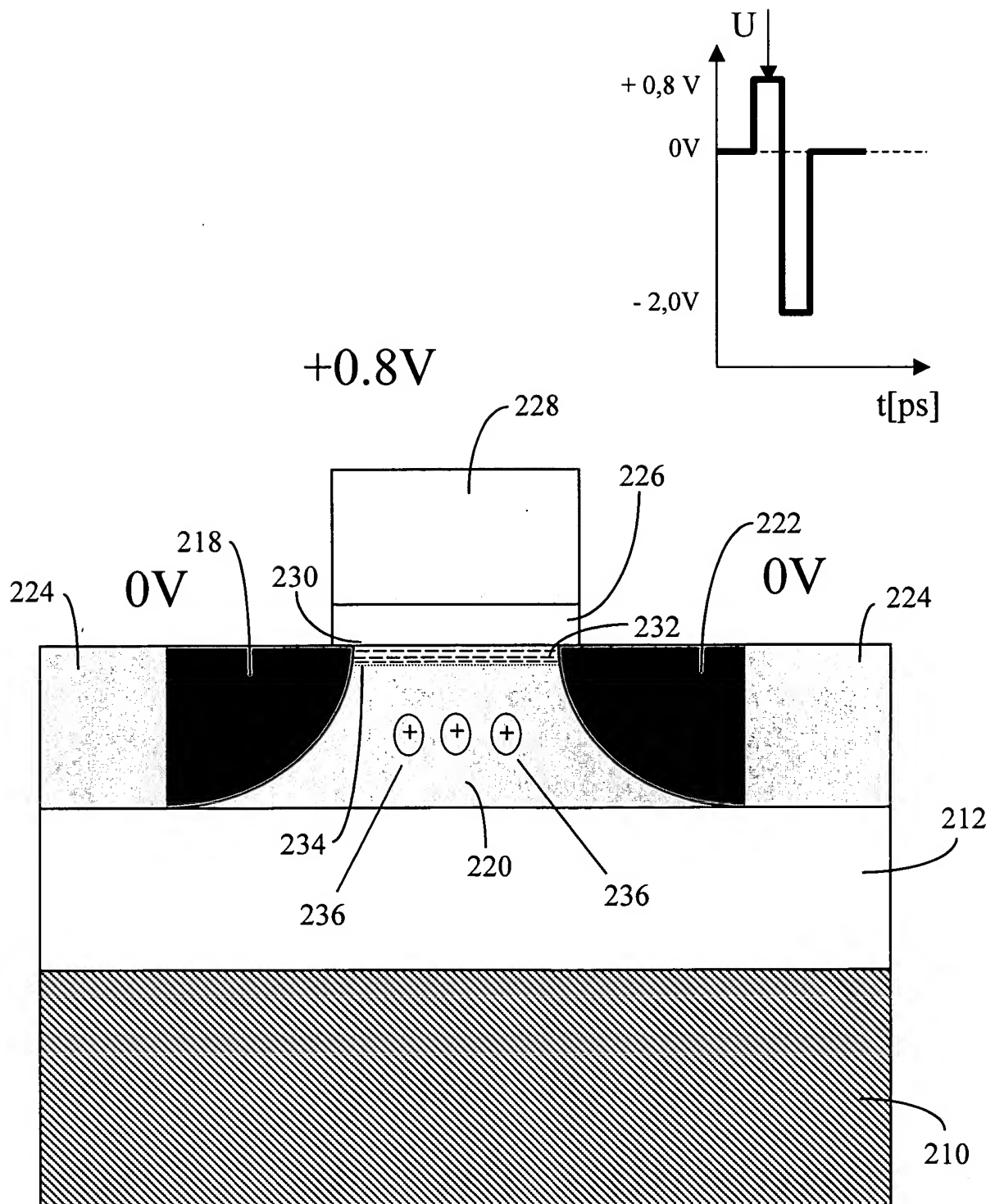


Fig. 7b

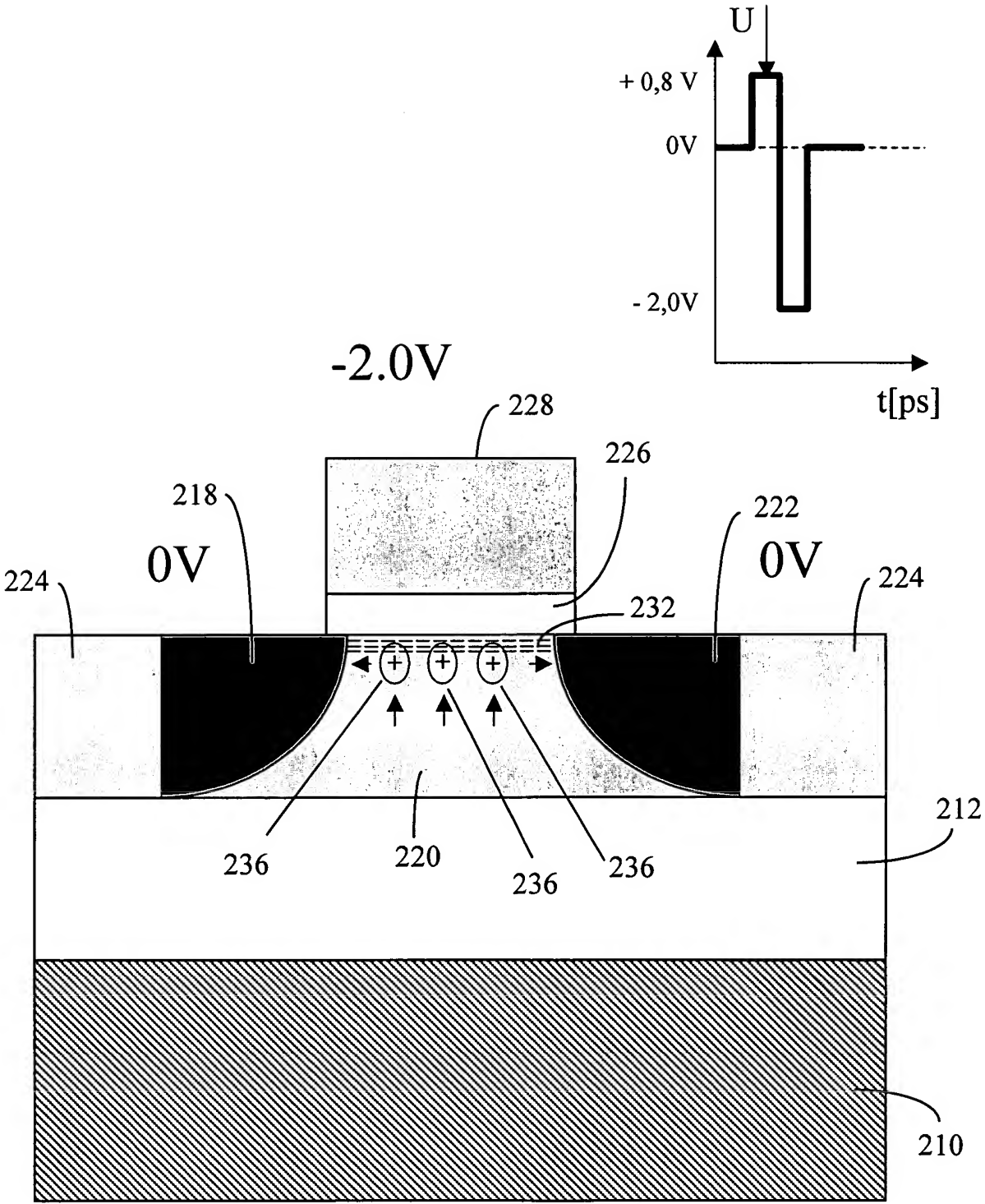


Fig. 7c

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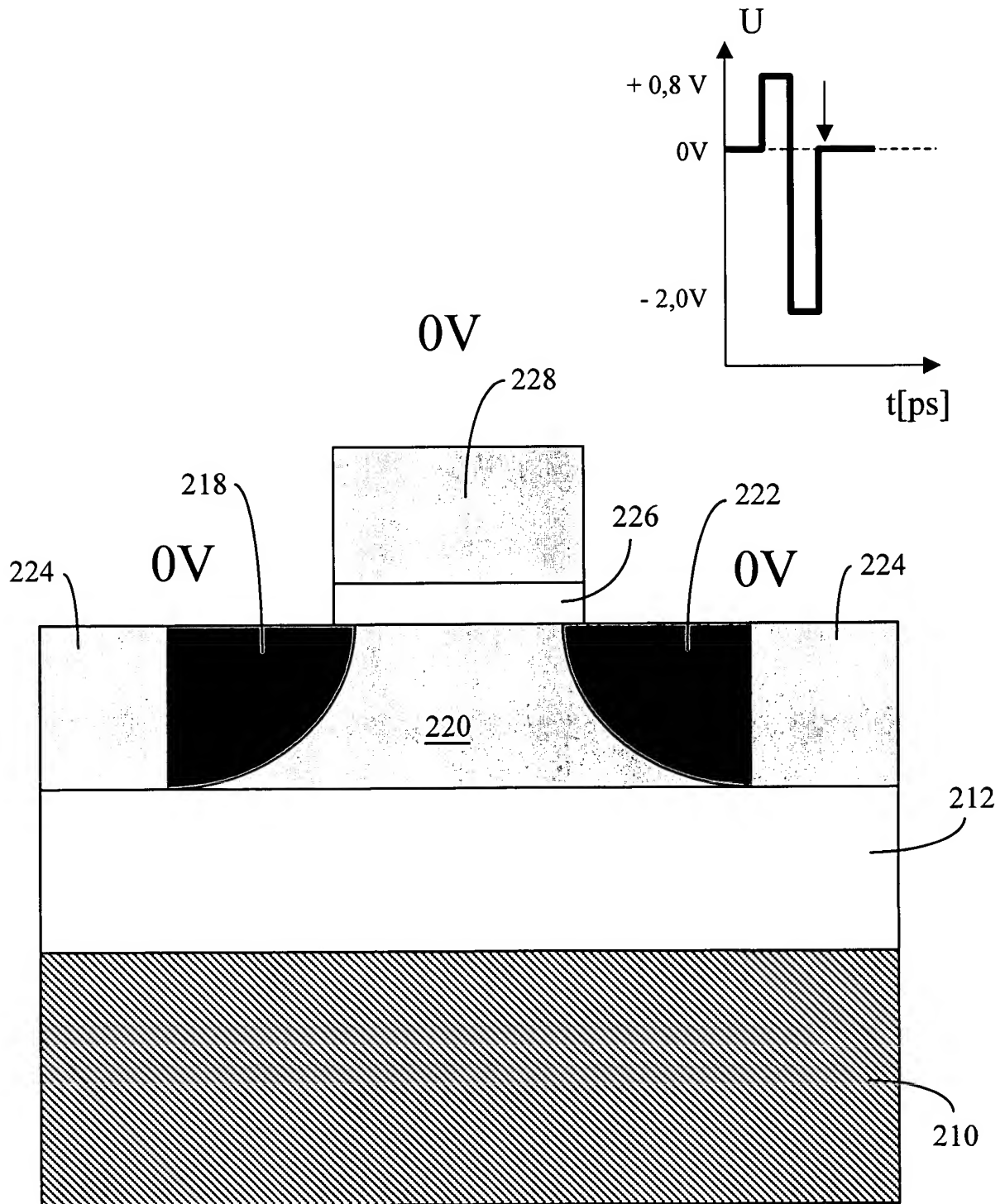


Fig. 7d

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**PD-SOI
NMOS**

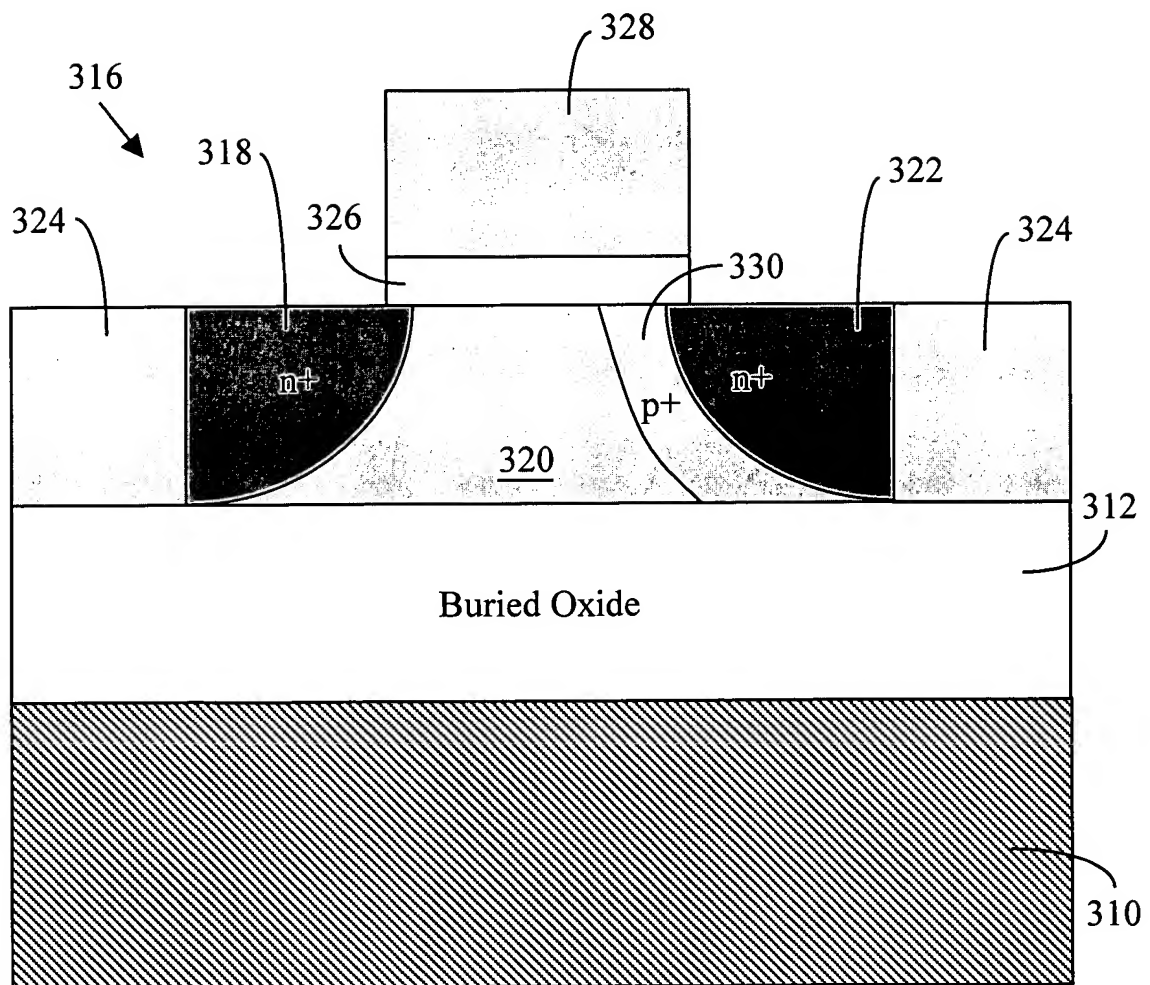


Fig. 8

Binary memory

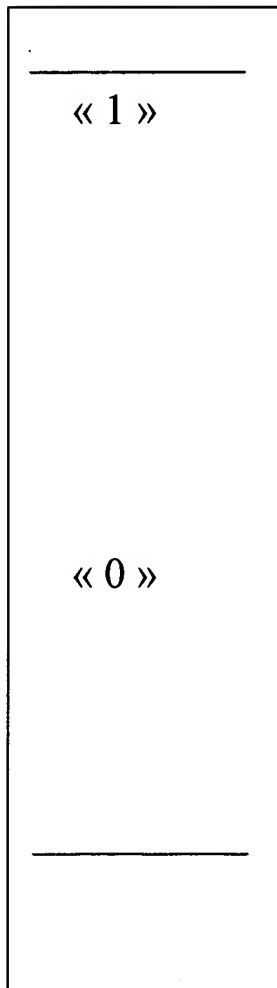


Fig. 10a

Multilevel memory

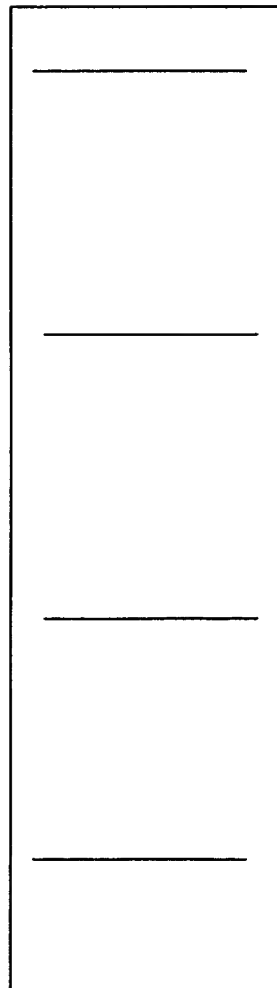


Fig. 10b

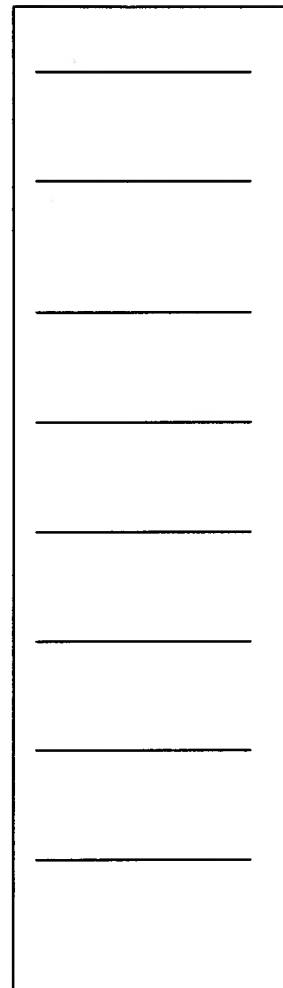


Fig. 10c

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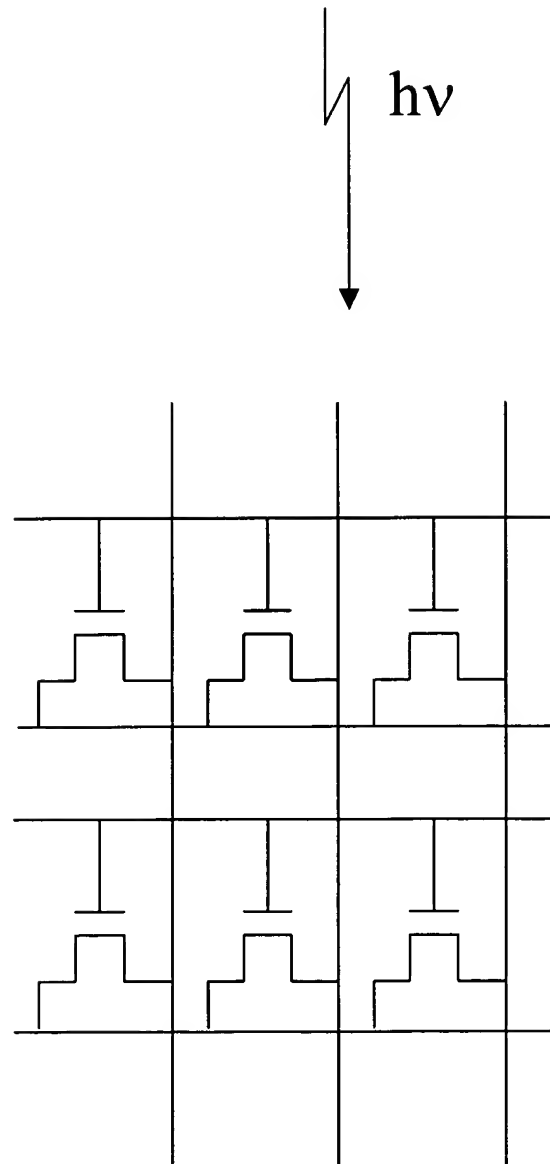


Fig. 18